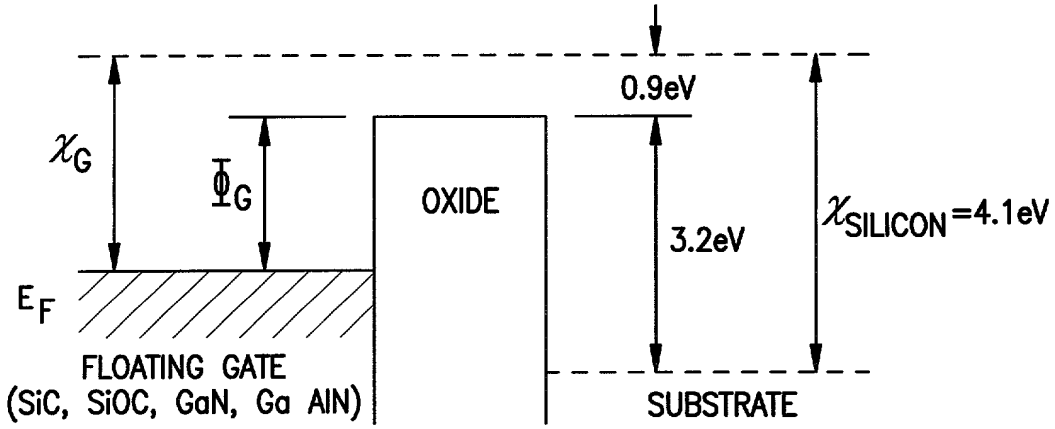


FIG. 1A
(PRIOR ART)

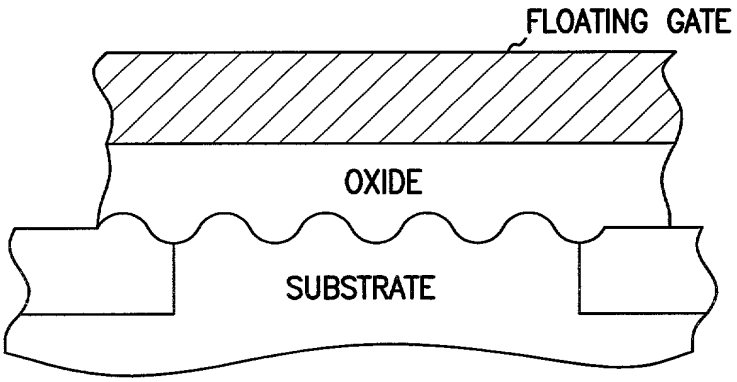


FIG. 1B
(PRIOR ART)

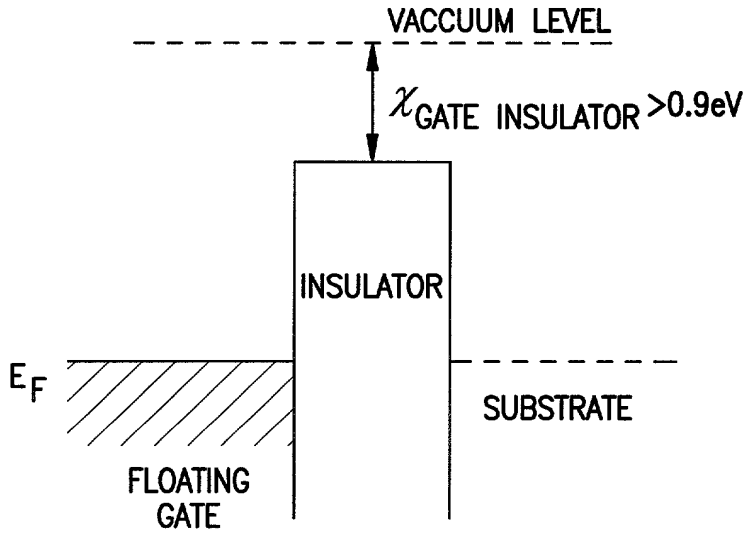


FIG. 1C
(PRIOR ART)

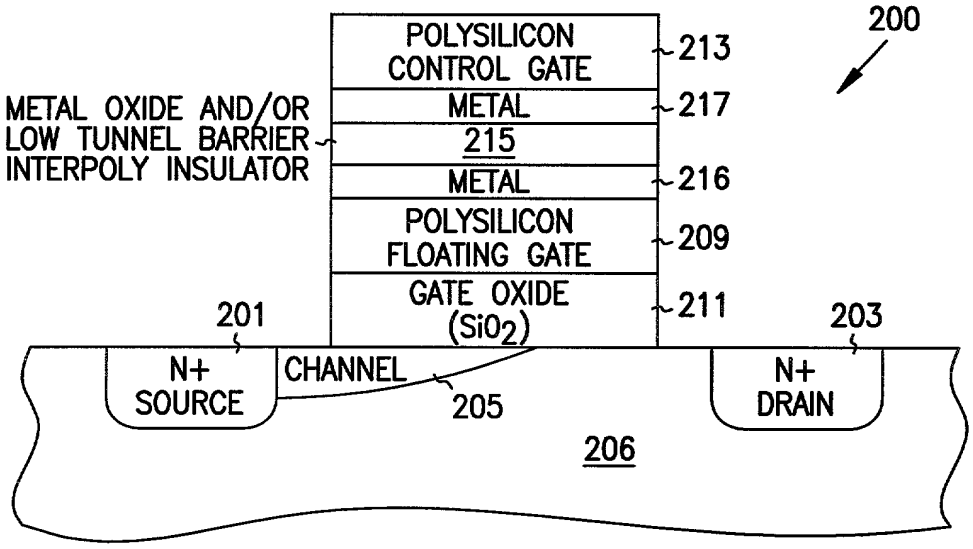


FIG. 2

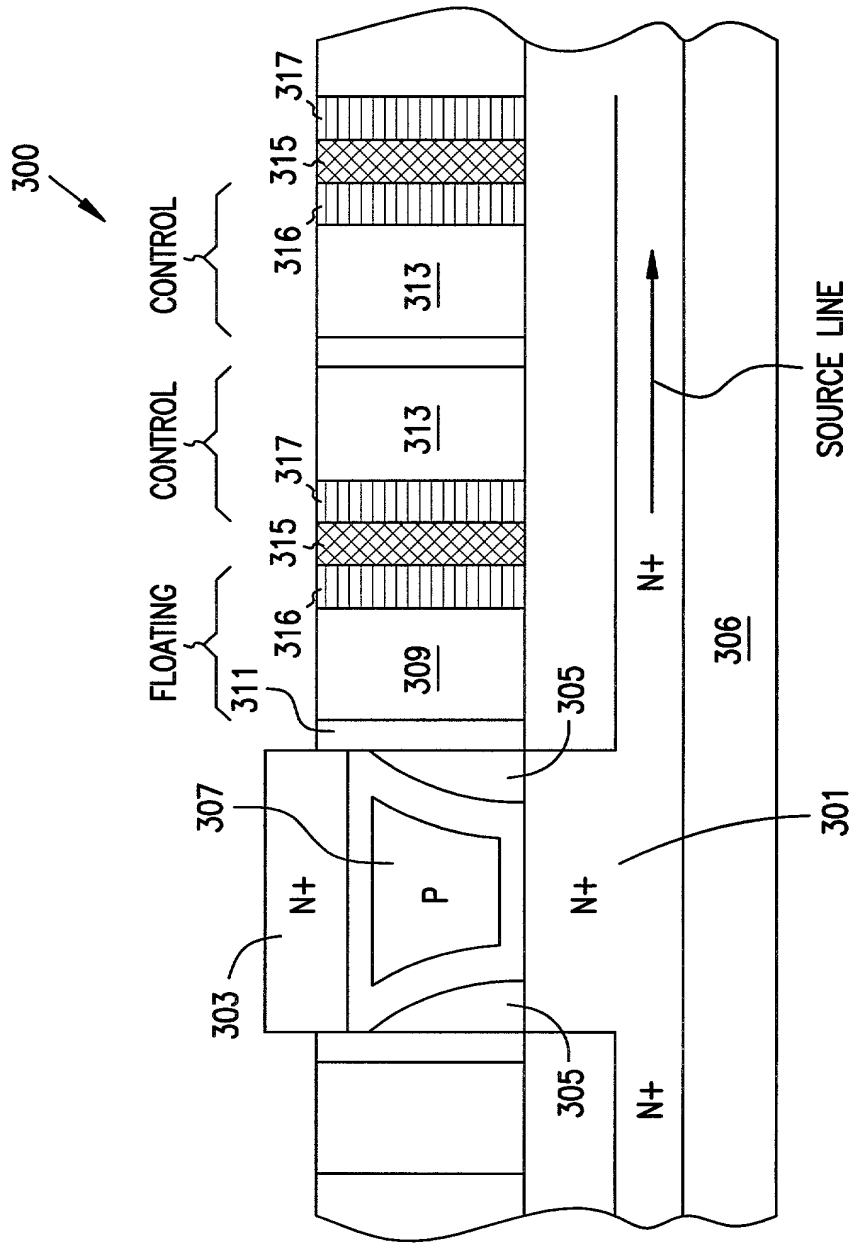

300
CONTROL
CONTROL
FLOATING
317
315
316
313
313
317
315
316
309
311
305
307
303
305
N+
P
N+
N+
306
301
SOURCE LINE

FIG. 3

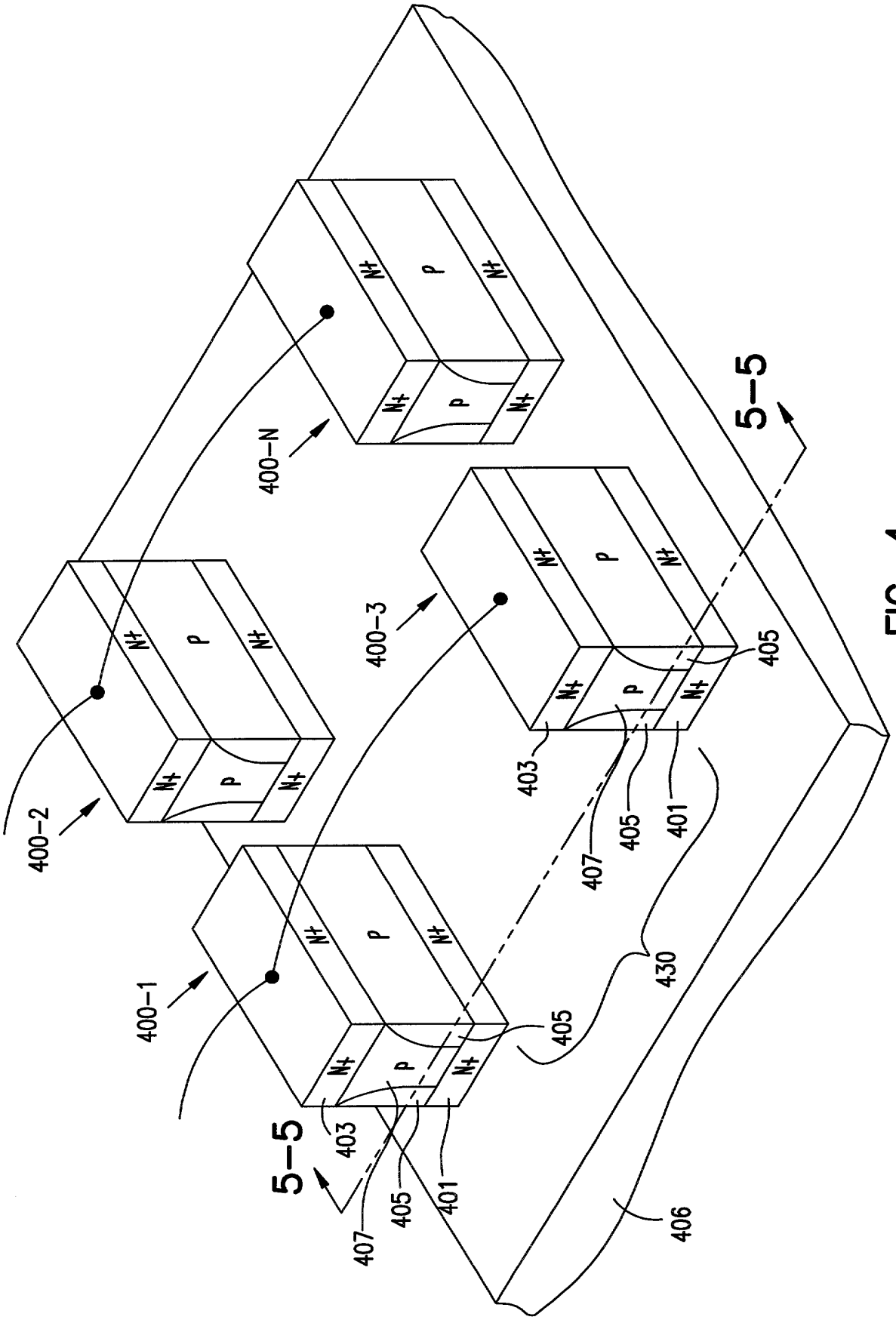


FIG. 4

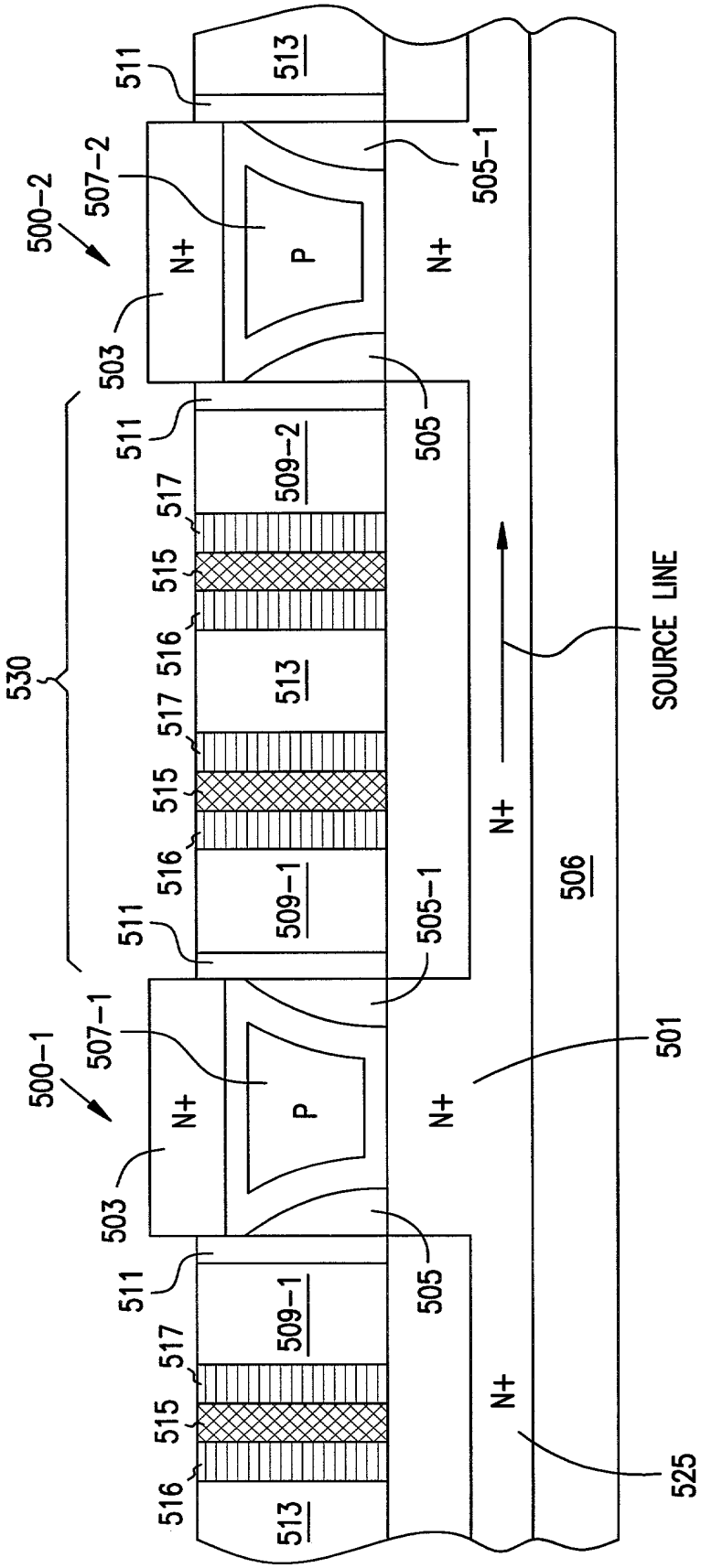

511
513
505-1
507-2
500-2
N+
P
N+
503
505
511
509-2
517
515
516
513
517
515
516
530
509-1
511
505-1
SOURCE LINE
N+
506
507-1
500-1
501
N+
P
N+
503
505
511
509-1
517
515
516
513
N+
525

FIG. 5A

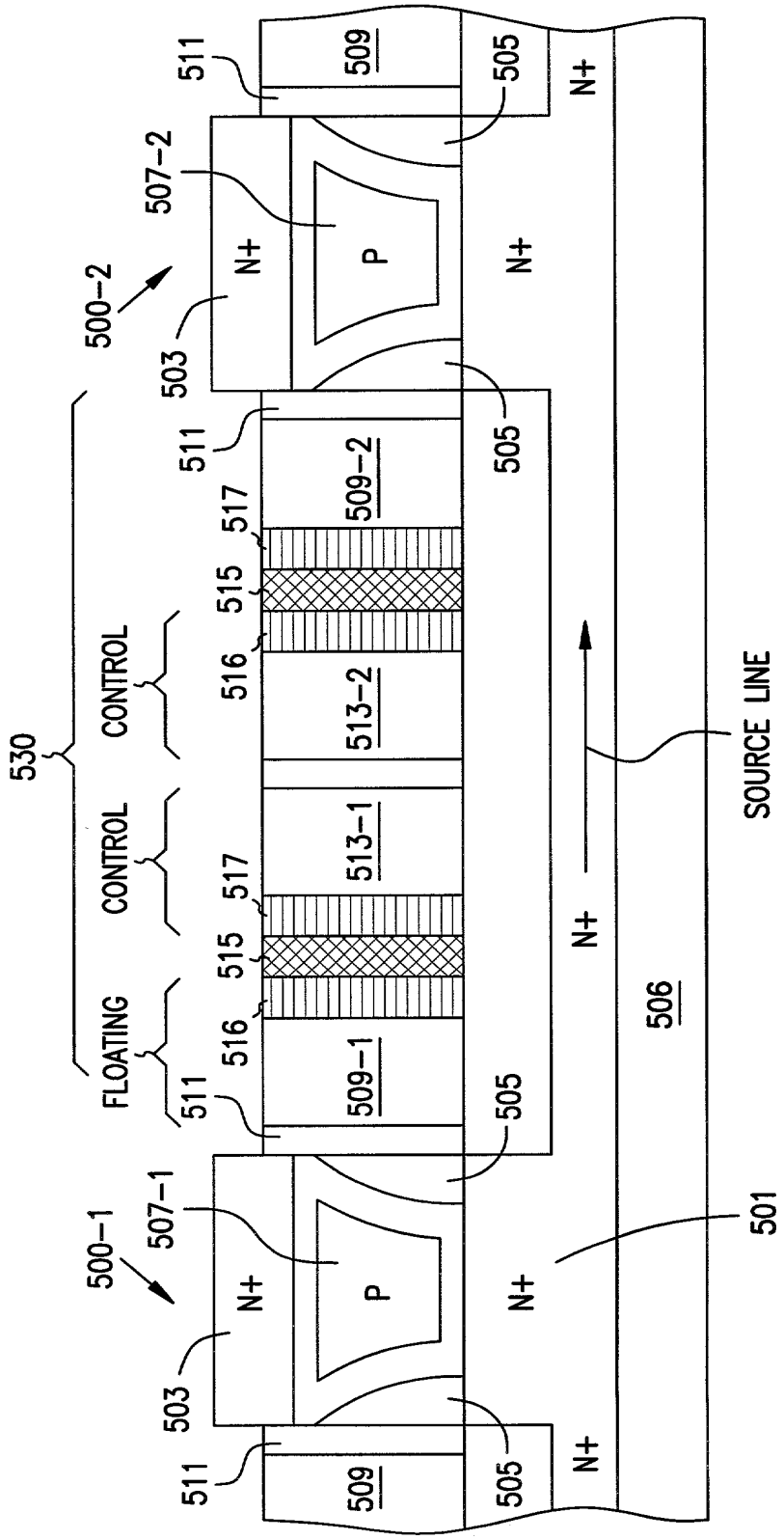

511
509
505
N+
507-2
500-2
503
P
N+
511
509-2
505
517
515
516
513-2
530
CONTROL
513-1
CONTROL
517
515
516
FLOATING
509-1
511
505
SOURCE LINE
N+
506
500-1
507-1
501
N+
P
N+
503
511
509
505
N+

FIG. 5B

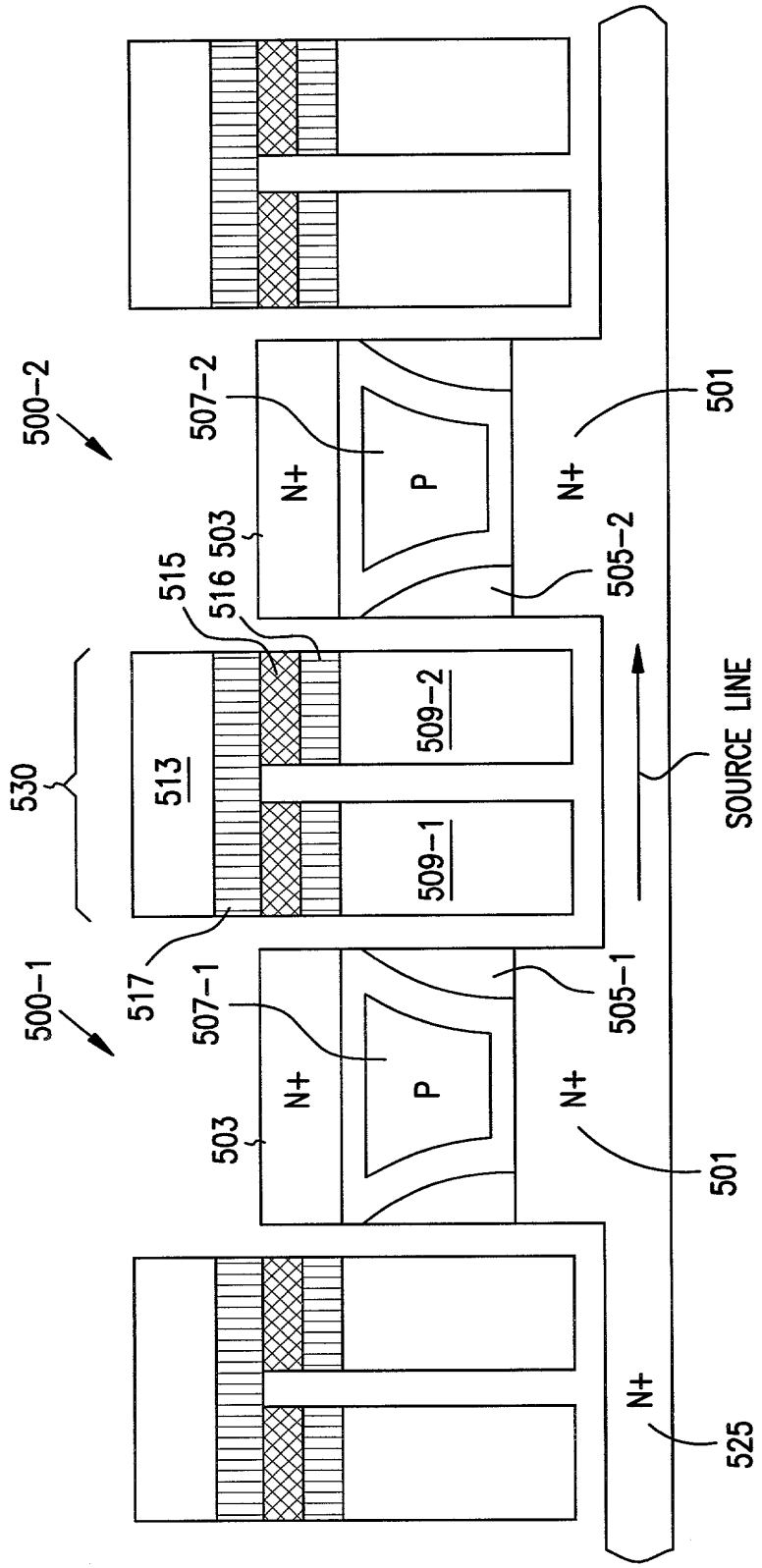

500-2
507-2
N+
P
N+
501
503
515
516
505-2
530
513
509-2
509-1
SOURCE LINE
517
500-1
507-1
505-1
N+
P
N+
503
501
N+
525

FIG. 5C

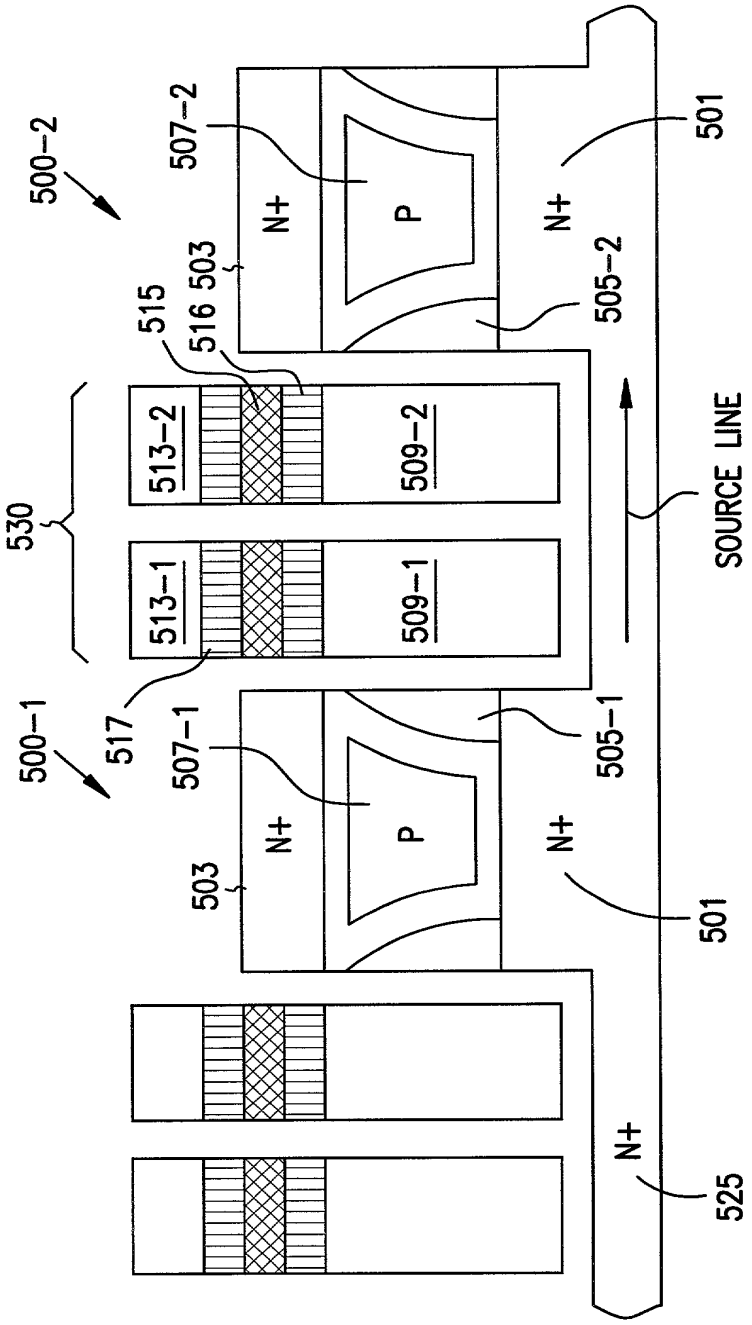

500-2
507-2
N+
P
N+
501
503
515
516
505-2
513-2
509-2
530
513-1
509-1
SOURCE LINE
500-1
517
507-1
505-1
N+
P
N+
503
501
N+
525

FIG. 5D

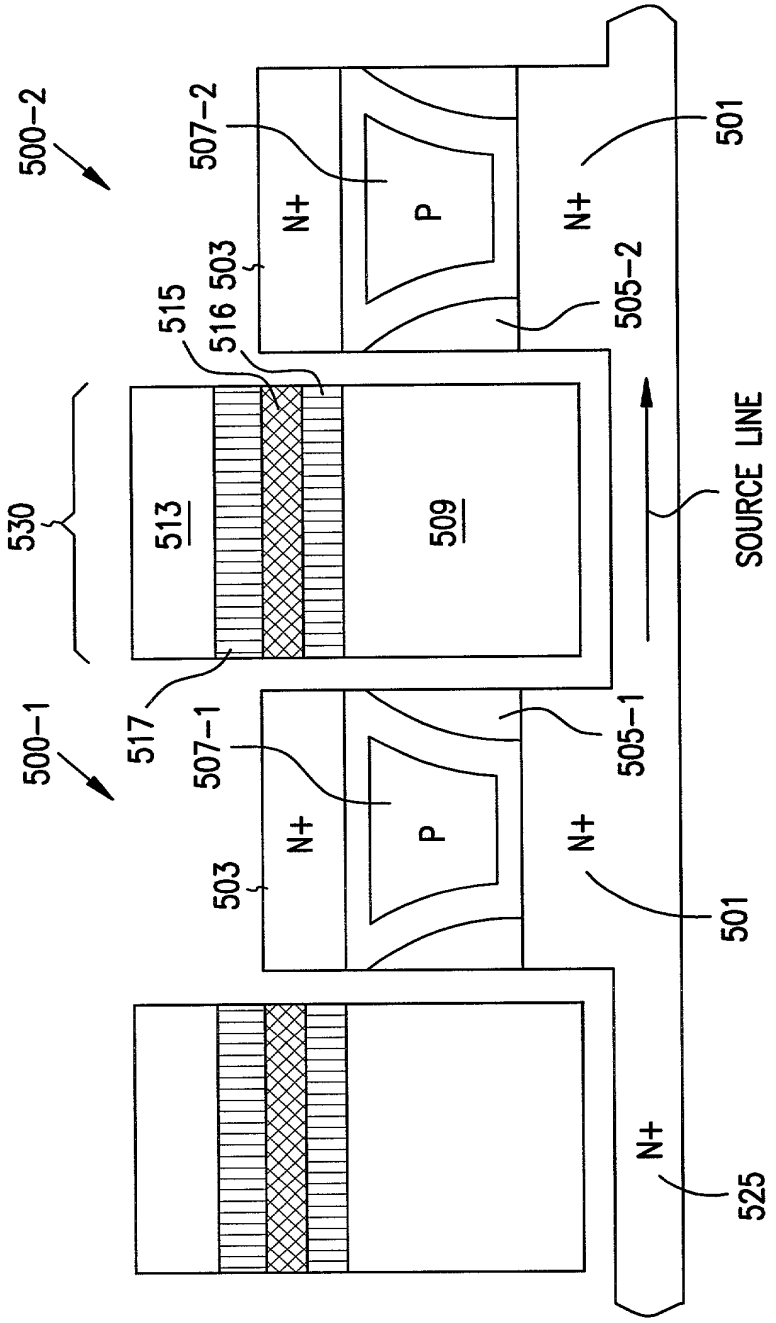

500-2
507-2
N+
P
N+
501
503
515
516
505-2
530
513
509
SOURCE LINE
517
500-1
507-1
505-1
N+
P
N+
503
501
N+
525

FIG. 5E

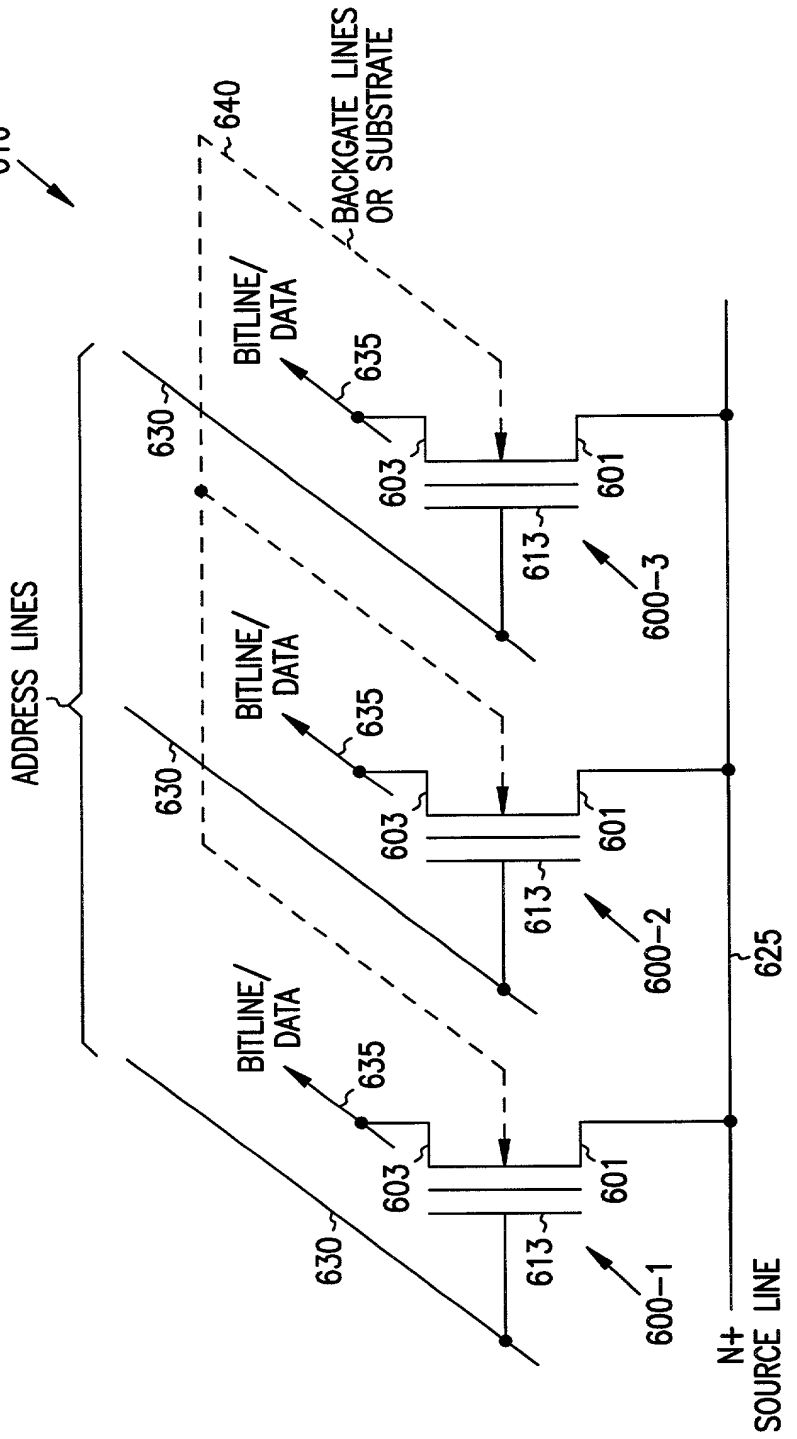

610
640
BACKGATE LINES OR SUBSTRATE
ADDRESS LINES
BITLINE/ DATA
635
630
603
601
613
600-3
600-2
600-1
625
N+ SOURCE LINE

FIG. 6A

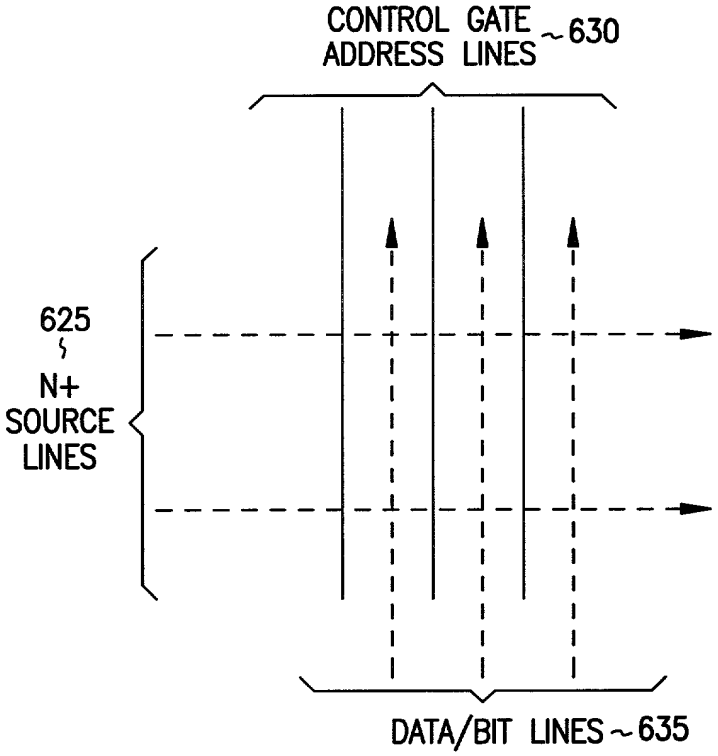

CONTROL GATE
ADDRESS LINES
630
625
N+
SOURCE
LINES
DATA/BIT LINES
635

FIG. 6B

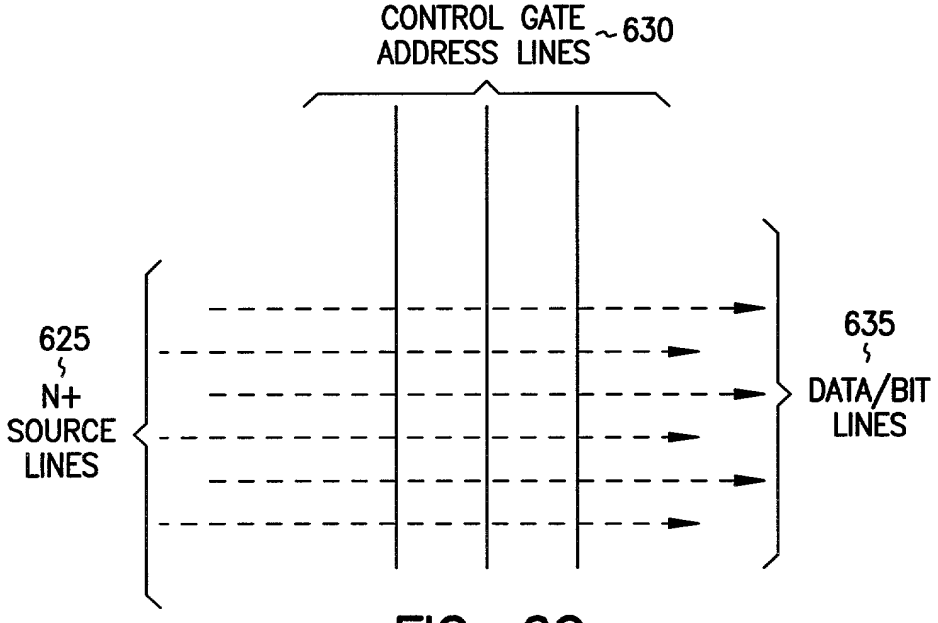

CONTROL GATE
ADDRESS LINES
630
625
N+
SOURCE
LINES
635
DATA/BIT
LINES

FIG. 6C

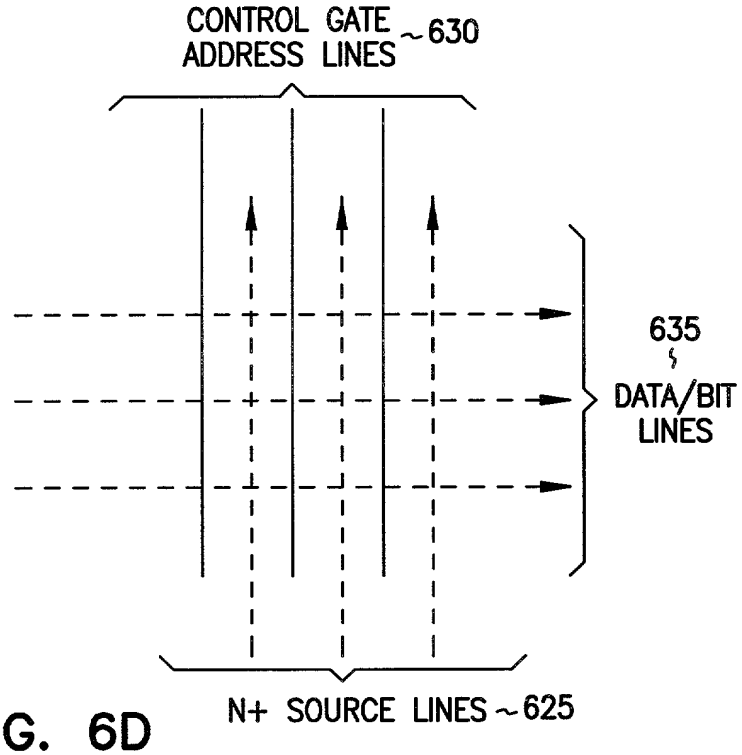

CONTROL GATE ADDRESS LINES ~630
635
DATA/BIT LINES
N+ SOURCE LINES ~625

FIG. 6D

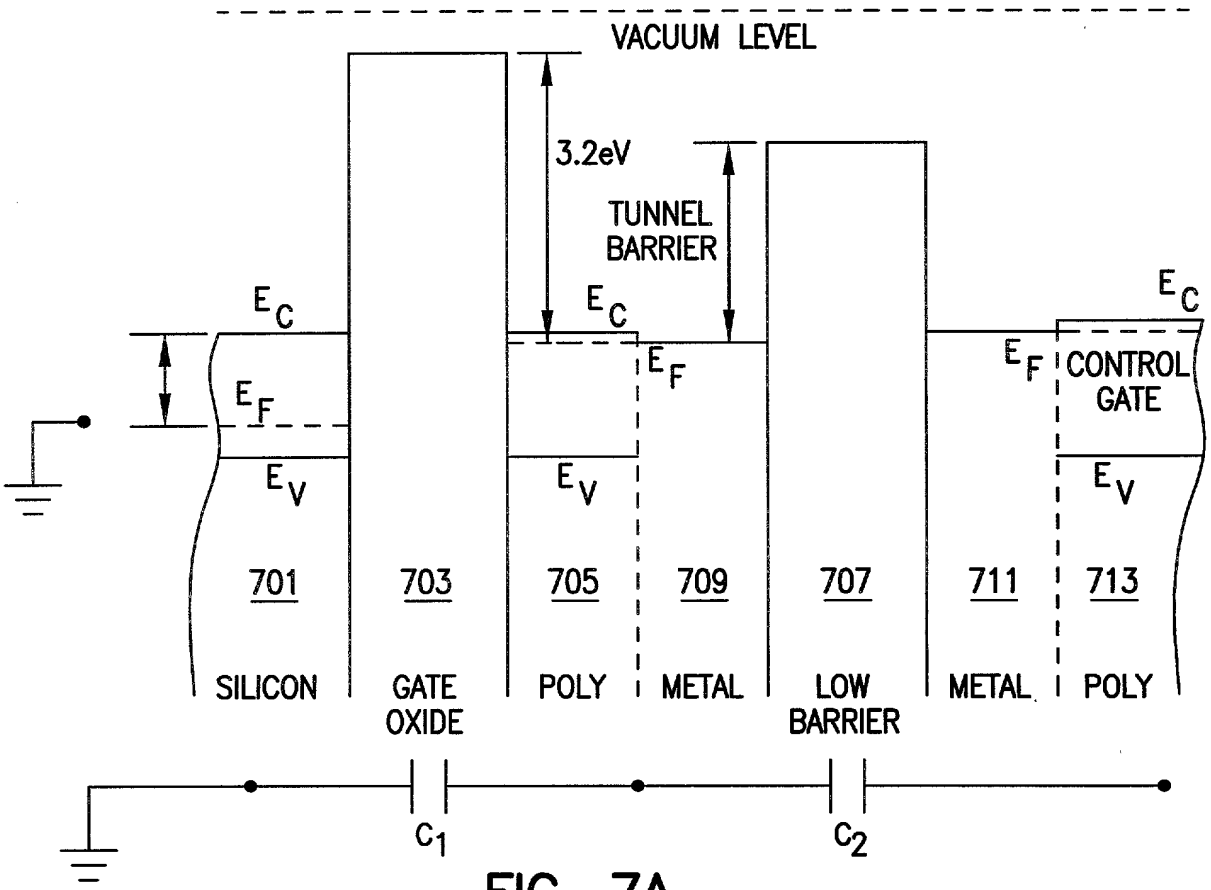
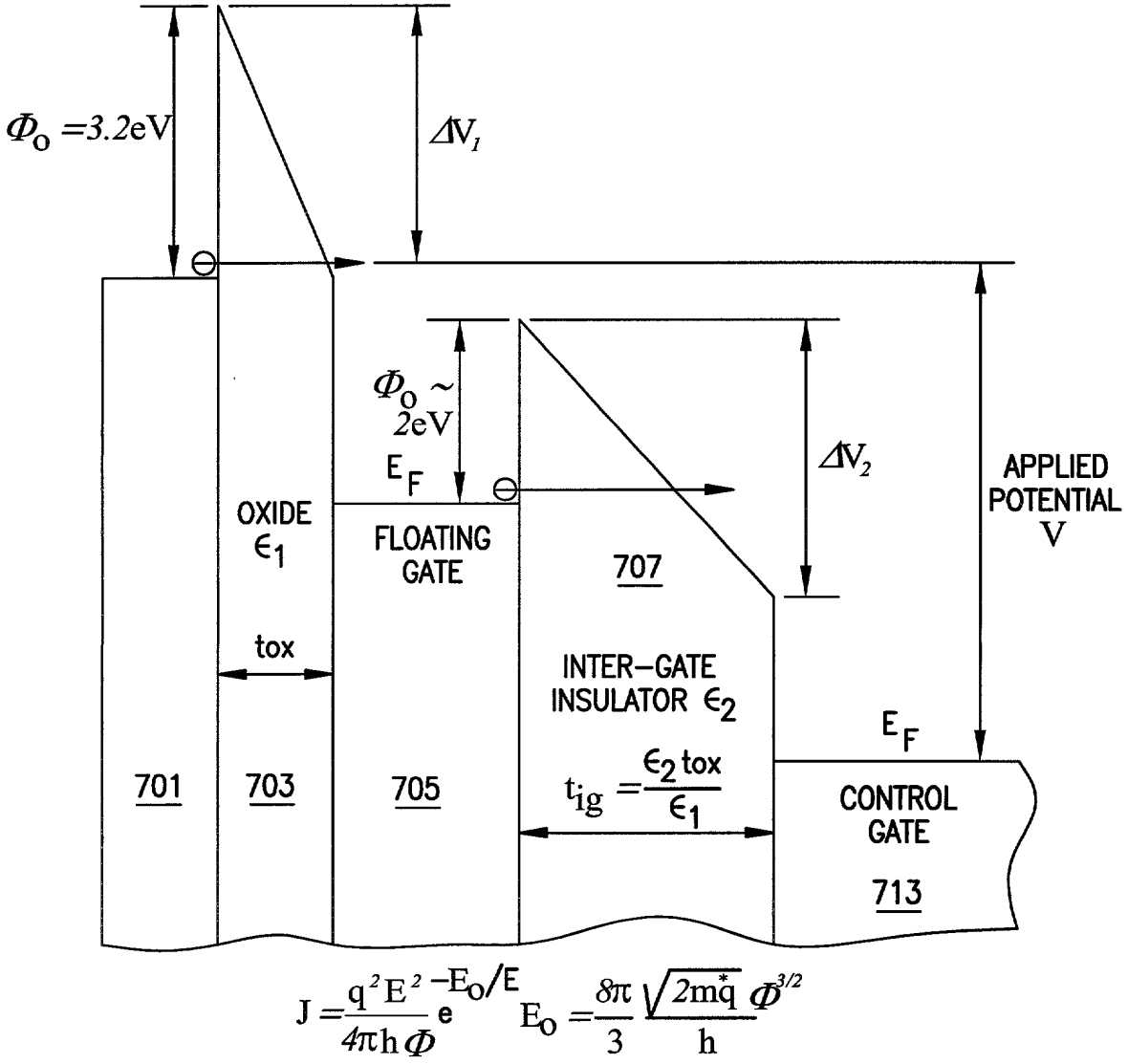

VACUUM LEVEL
3.2eV
TUNNEL BARRIER
E_C
E_F
E_V
CONTROL GATE
701
703
705
709
707
711
713
SILICON
GATE OXIDE
POLY
METAL
LOW BARRIER
METAL
POLY
C_1
C_2

FIG. 7A



$$J = \frac{q^2 E^2}{4\pi h \Phi} e^{-E_o/E} \qquad E_o = \frac{8\pi}{3} \frac{\sqrt{2m_q^*}}{h} \Phi^{3/2}$$

FIG. 7B

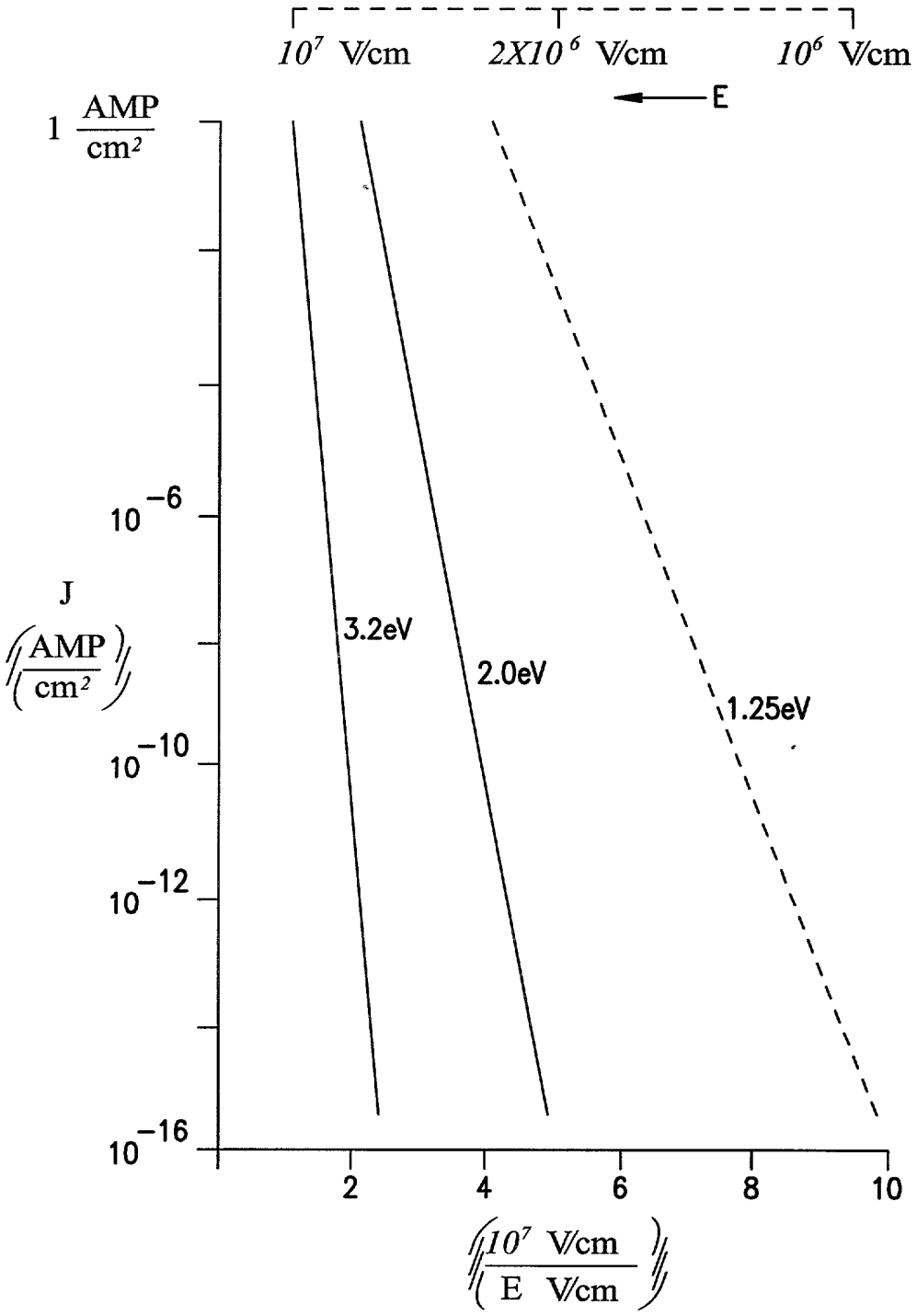

10^7 V/cm
$2X10^6$ V/cm
10^6 V/cm
E
1 AMP/cm²
10^{-6}
J (AMP/cm²)
10^{-10}
10^{-12}
10^{-16}
3.2eV
2.0eV
1.25eV
2
4
6
8
10
(10^7 V/cm / E V/cm)

FIG. 7C

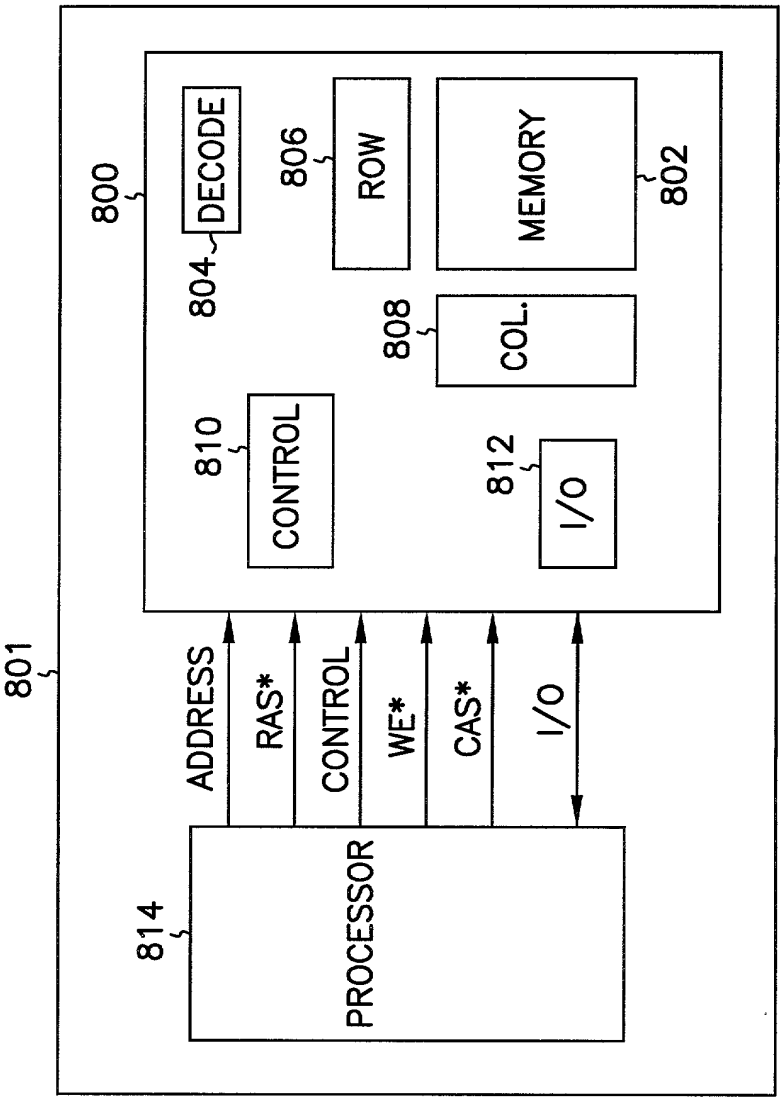

801
800
DECODE
804
806
ROW
MEMORY
802
808
COL.
810
CONTROL
812
I/O
ADDRESS
RAS*
CONTROL
WE*
CAS*
I/O
814
PROCESSOR

FIG. 8